REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-16 are currently pending in the present application. By way of this reply, claims 1, 7, 12, and 16 have been amended.

II. Claim Amendments

Claim 1 has been amended to clarify that the error checking circuit is electrically disposed between the first memory bank and the multiplexer. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 2 of the present application.

Claim 7 has been amended to clarify that the means for error checking is electrically disposed between the first memory device and the selection means. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 2 of the present application.

Claim 12 has been amended to clarify that checking the data occurs electrically between reading data from the desired location of the first memory bank and outputting data from one of the first memory bank and the second memory bank to the bus. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 2 of the present application.

Claim 16 has been amended to clarify that the parity checking circuit is electrically disposed between the first static random access memory bank and the multiplexer. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 2 of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1-4, 6-10, and 12-16 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,611,042 issued to Lordi (hereinafter "Lordi"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a design by which errors in a memory system may be reduced. *See* Specification, Abstract. With reference to the exemplary embodiment of the present invention shown in Figure 2 of the present application, a memory system is provided with redundant memory banks **21**, **23**. Data read from each of the memory banks **21**, **23** propagates to an input of a multiplexer **27**. A select input **29** to the multiplexer **27** is controlled by an error checking circuit **25** that checks for errors in the data read from memory bank **21**. If no errors are present in the data read from memory bank **21**, the error checking circuit **25** controls the select input **29** to the multiplexer **27** such that data read from memory bank **21** passes from the input of the multiplexer **27** to an output bus **31**. Alternatively, if there are errors present in the data read from memory bank **21**, the error checking circuit **25** controls the select input **29** to the multiplexer **27** such that data read from memory bank **23** passes from the input of the multiplexer **27** to the output bus **31**.

Further, as shown in Figure 2 of the present application, the error checking circuit **25** is electrically disposed between memory bank **21** and the multiplexer **27**. Accordingly, independent claim 1 of the present application has been amended to clarify that the error checking circuit is electrically disposed between the first memory bank and the multiplexer. Independent claims 7, 12, and 16 of the present application have been respectively amended with similar means-plus function, method, and apparatus limitations.

Lordi, in contrast to the present invention, fails to disclose all the limitations of amended independent claims 1, 7, 12, and 16 of the present application. As shown in Figures 2, 4, and 6 of Lordi, the purported error checking circuit **50** is positioned between the purported multiplexer **40** and a microcontroller **20**. The purported error checking circuit **50** receives parity bits $\mathbf{P_1}$ and $\mathbf{P_2}$ from the purported first memory bank **10** and the purported second memory bank **11**, respectively. Thus, the purported error checking circuit **50** does not directly check for errors in the stream of data read from either of the purported memory banks **10, 11** that also serve as an input to the purported multiplexer **40**. Instead, the purported error checking circuit **50** receives bits indicative of error directly from the purported memory banks **10, 11**. In other words, data read from the purported memory banks **10, 11** never serve (and are electrically incapable of serving) as an input to the purported error checking circuit **50**. Therefore, the purported error checking circuit **50** is not, and cannot be, electrically disposed between the either of the purported memory banks **10, 11** and the purported multiplexer **40** as required by the claimed invention.

On the other hand, in the present invention as exemplarily shown in Figure 2 of

the present application, the data read from the memory bank **21** serves as both an input to the error checking circuit **25** and the multiplexer **27**. In such a manner, the error checking circuit **25** is electrically *disposed between* the memory bank **21** and the multiplexer **27** as recited in amended independent claim 1 of the present application. Lordi fails at least to disclose or otherwise teach such a limitation and the corresponding means-plus function, method, and apparatus limitations required by amended independent claims 7, 12, and 16 of the present application, respectively.

In view of the above, Lordi fails to show or suggest the present invention as recited in amended independent claims 1, 7, 12, and 16 of the present application. Thus, amended independent claims 1, 7, 12, and 16 of the present application are patentable over Lordi. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Rejection(s) Under 35 U.S.C § 103

Claims 5 and 11 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lordi in view of U.S. Patent No. 6,237,124 issued to Plants (hereinafter "Plants"). For the reasons set forth below, this rejection is respectfully traversed.

Like Lordi discussed above, Plants fails to disclose all the limitations of amended independent claims 1 and 7 of the present application. Plants, which is directed to a technique for detecting error in stored data (*see* Plants, Abstract), discloses in Figure 4 of Plants a cyclical redundancy checking (CRC) circuit **40** that checks for single event upset (SEU) occurrences on an output from a multiplexer **42** that inputs data read from an

SRAM (located in FPGA core **10** as shown in Figure 5A of Plants). *See* Plants, column 4, lines 15 – 29. Thus, Plants necessarily cannot disclose an error checking circuit *disposed between* a memory bank and a multiplexer as required by amended independent claim 1 of the present application. Similarly, Plants fails to disclose the corresponding means-plus function limitation of amended independent claim 7 of the present application. Accordingly, Plants fails to disclose those limitations of amended independent claims 1 and 7 of the present application not disclosed or taught by Lordi.

In view of the above, Lordi and Plants, whether considered separately or in combination, fail to show or suggest the present invention as recited in amended independent claims 1 and 7 of the present application. Thus, amended independent claims 1 and 7 of the present application are patentable over Lordi and Plants. Dependent claims 5 and 11 are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.053002;P5039).

Respectfully submitted,

Date: 2/6/04

for Jonathan P. Osha, Reg. No. 33,986 48,885

ROSENTHAL & OSHA L.L.P.
1221 McKinney Street, Suite 2800
Houston, TX 77010

Telephone: (713) 228-8600
Facsimile: (713) 228-8778

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